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**INFORMATION DISCLOSURE
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Complete If Known

Application Number	09/917,257
Filing Date	July 27, 2001
First Named Inventor	Rumynin, Dmitriy RECEIVED
Group Art Unit	2121
Examiner Name	Unknown MAR 20 2003

Sheet 1 of 2

Attorney Docket No: 1365.051US1

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T R A D E M A R K C E N T E R

US PATENT DOCUMENTS

Examiner Initials*	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	Filing Date If Appropriate
	US-3,634,658	01/11/1972	Brown, Richard	235	92LG	03/19/1970
	US-3,757,098	09/04/1973	Wright, Carl	235	175	05/12/1972
	US-4,607,176	08/19/1986	Burrows, James, et al.	307	449	08/22/1984
	US-5,095,457	03/10/1992	Ho-sun Jeong	364	758	02/01/1990
	US-5,175,862	12/29/1992	Phelps, Andrew, et al.	395	800	06/11/1990
	US-5,524,082	06/04/1996	Horstmann, P., et al.	364	489	06/28/1991
	US-5,995,029	11/30/1999	Ryu, Myung	341	101	10/29/1997
	US-6,023,566	02/08/2000	Belkhale, K., et al.	395	500.03	04/14/1997

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	T ²
	EP-0168650	01/22/1986	Darringer, J., et al.	G06F	15/60	
	EP-0309292	03/29/1989	Nishiyama, T., et al.	G06F	15/60	
	EP-0442356	08/21/1991	Chang, Yen C., et al.	G06F	7/50	
	EP-0741354	11/06/1996	Ichikawa, Takeshi	G06F	7/60	
	FR-2475250	08/07/1981	Houdard, Jean-Pierre, et al.	606F	7/38	With English Abstract
	GB-2016181	09/19/1979	Gajski, Daniel, et al.	606F	7/39	
	GB-2062310	05/20/1981	Ohhashi, Masahide, et al.	606F	7/52	
	GB-2365636	02/20/2002	Rumynin, D., et al.	G06F	7/60	
	GB-2365637	02/20/2002	Rumynin, D., et al..	G06F	7/60	
	WO-99/22292	05/06/1999	Verbauwheide, Ingrid	606F	7/52	
	WO-02/12995	02/14/2002	Meulemans, P., et al.	G06F	7/00	

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		BOOTH, ANDREW, "A Signed Binary Multiplication Technique", <u>Oxford University Press</u> , Reprinted from Q.J. Mech. Appl. Math. 4:236-240, (1951), pp. 100-104	
		CHAKRABORTY, S., et al., "Synthesis of Symmetric Functions for Path-Delay Fault Testability", <u>12th International Conference on VLSI Design</u> , (1999), pp. 512-517	
		DADDA, L., "On Parallel Digital Multipliers", <u>Associazione Elettronica ed Elettronica Italiana</u> , Reprinted from Alta Freq. 45:574-580, (1976), pp. 126-132	
		DADDA, L., "Some Schemes For Parallel Multipliers", <u>Associazione Elettronica ed Elettronica Italiana</u> , Reprinted from Alta Freq. 34:349-356,	

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11/17/04

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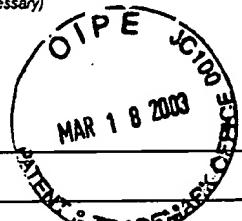
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Group Art Unit	2121
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		(1965), pp. 118-125	
		DEBNATH, D., "Minimization of AND-OR-EXOR Three-Level Networks with AND Gate Sharing", <u>IEICE Trans. Inf. & Syst.</u> , Vol. E80-D, No. 10, (1997), pp. 1001-1008	
		DRECHSLER, R., et al., "Sympathy: Fast Exact Minimization of Fixed Polarity Reed-Muller Expressions for Symmetric Functions", <u>IEEE</u> , (1995), pp. 91-97	
		DRECHSLER, R., et al., "Sympathy: Fast Exact Minimization of Fixed Polarity Reed-Muller Expressions for Symmetric Functions", <u>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</u> , Vol. 16, No. 1, (1997), pp. 1-5	
		FLEISHER, H., "Combinatorial Techniques for Performing Arithmetic and Logical Operations", <u>IBM Research Center, RC-289, Research Report</u> , (July 18, 1960), pp. 1-20	
		FOSTER, CAXTON, et al., "Counting Responders in an Associative Memory", <u>The Institute of Electrical and Electronics Engineers, Inc.</u> , Reprinted, with permission, from <u>IEEE Trans. Comput. C-20:1580-1583</u> , (1971), pp. 86-89	
		HO, I., et al., "Multiple Addition by Residue Threshold Functions and Their Representation By Array Logic", <u>The Institute of Electrical and Electronics Engineers, Inc.</u> , Reprinted, with permission from <u>IEEE Trans. Comput. C-22:762-767</u> , (1973), pp. 80-85	
		JONES, ROBERT, et al., "Parallel Counter Implementation", <u>IEEE</u> , (1992), pp. 381-385	
		NIENHAUS, H., "Efficient Multiplexer Realizations of Symmetric Functions", <u>IEEE</u> , (1981), pp. 522-525	
		OKLOBDZIJA, V.G., et al., "Improving Multiplier Design by Using Improved Column Compression Tree and Optimized Final Adder in CMOS Technology", <u>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</u> , Vol. 3, No. 2, (1995), pp. 292-301	
		SWARTZLANDER, JR., EARLE, "Parallel Counters", <u>Institute of Electrical and Electronic Engineers, Inc.</u> , Reprinted, with permission from <u>IEEE Trans. Comput. C-22:1021-1024</u> , (1973), pp. 90-93	
		VASSILIADIS, S., et al., "7/2 Counters and Multiplication with Threshold Logic", <u>IEEE</u> , (1997), pp. 192-196	
		WALLACE, C., "A Suggestion for a Fast Multiplier", <u>IEEE Transactions on Electronic Computers</u> , (1964), pp. 14-17	
		ZURAS, D, et al., "Balanced Delay Trees and Combinatorial Division in VLSI", <u>IEEE Journal of Solid State Circuits</u> , SC-21, IEEE Inc, New York, Vol. SC-21, No. 5, (1986), pp. 814-819	

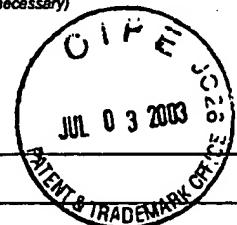
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US PATENT DOCUMENTS

Examiner Initials*	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	Filing Date if Appropriate
	US-4,399,517	08/16/1983	Niehaus, Jeffrey A., et al.	364	784	03/19/1981
	US-5,095,547	03/17/1992	Kerns, Carol S.	2	160	06/13/1991
	US-5,187,679	02/16/1993	Vassiliadis, Stamatis, et al.	364	786	06/05/1991
	US-5,325,320	06/28/1994	Chiu, Chiao-Er A.	364	760	05/01/1992
	US-5,343,417	08/30/1994	Flora, Laurence P.	364	758	11/20/1992
	US-5,497,342	03/05/1996	Mou, et al.	364	786	11/09/1994
	US-6,490,608	12/03/2002	Zhu, Jay	708	626	12/09/1999

FOREIGN PATENT DOCUMENTS

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OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

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		GOTO, et al., "A 54 x 54-b Regularly Structured Tree Multiplier", <u>IEEE Journal of Solid-State Circuits</u> , Vol 27, No. 9, (Sept. 1992), 1229-1236	
		HEKSTRA, et al., "A Fast Parallel Multiplier Architecture", <u>IEEE International Symposium on Circuits and Systems</u> , Institute of Electrical and Electronic Engineers, c1977-c1996, 20v. :ill. :28cm. (1992), 2128-2131	

EXAMINER

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DATE CONSIDERED

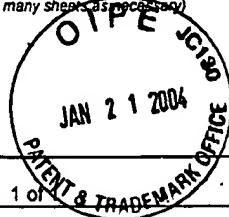
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Application Number	09/917257
Filing Date	July 27, 2001
First Named Inventor	Rumynin, Dmitriy
Group Art Unit	2121 2124
Examiner Name	Unknown

Attorney Docket No: 1365.051US1

US PATENT DOCUMENTS

Examiner Initials*	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	Filing Date If Appropriate
	US-5,964,827	10/12/1999	Ngo, Hung C., et al.	708	710	11/17/1997

FOREIGN PATENT DOCUMENTS

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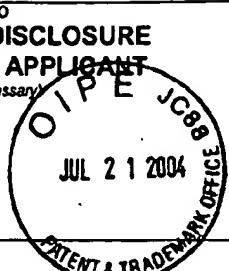
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<i>[initials]</i>	US-6,175,852	01/16/2001	Dhong, S. H., et al.	708	712	07/13/1998
<i>[initials]</i>	US-6,269,386	07/31/2001	Siers, S. E., et al.	708	710	10/14/1998

FOREIGN PATENT DOCUMENTS

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<i>[initials]</i>		BEDRIJ, O. J., "Carry-Select Adder", IRE Trans., EC-11, (June 1962),340-346	
<i>[initials]</i>		KNOWLES, S. , "A Family of Adders", Proc. 14th IEEE Symp. on Computer Arithmetic, (1999),30-34	
<i>[initials]</i>		KOGGE, P. M., et al., "A Parallel Algorithm for the Efficient Solution of a General Class of Recurrence Equations", IEEE Trans. Computers, Vol. C-22, No. 8, (Aug. 1973),786-793	
<i>[initials]</i>		LADNER, RICHARD E., et al., "Parallel Prefix Computation", Journal of ACM, Vol. 27, No. 4, (Oct. 1980),831-838	
<i>[initials]</i>		LING, HUEY , "High-Speed Binary Adder", IBM Journal of Research and Development, Vol. 25, No. 3, (1981),156-166	
<i>[initials]</i>		SKLANSKY, J., "Conditional-Sum Addition Logic", IRE Trans., EC-9, (June 1960),226-231	
<i>[initials]</i>		WEINBERGER, A., et al., "A Logic for High-Speed Addition", Nat. Bur. Stand. Circ., 591, (1958),3-12	

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